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Course: COM219

**HOMEWORK 6**

Question 3:

1. 4x3 memory has 4 words, each store 3 data bits

→ To make 4x12 memory (4 words, each store 12 bits), need in total **four** 4x3 memory arrange in a row

→ To make 16x12 memory (16 words, each store 12 bits), need in total **four** 4x12 memory arrange in one column

→ To make 16x12 memory, need 4x4 = 16 4x3 chips

16x12 memory can store 16x12 = 192 bits → need 192 D FFs

1. Capacity = 25 x 210 = 215 bits

→ # cells: 215/16 = 211 = 2048 cells

→ Number of address pins: 11

Cell size = 16-bit → Number of data pins = 16

1. CPU has 32-bit data bus

→ Size of address space, in locations: 232 = 4,294,967,296 = 4GB address space.

1. 20-bit address line → 220 different addresses

Data bus size = 16 bit → Each address can store 16 bits = 2 bytes of data

→ Maximum addressable memory: 220 x 2 = 2MB

1. Number of addresses needed to be filled: BFFFF – 30000 = 8FFFF = 58982310

Each address store 16 bits data → Memory capacity = 589823 x 16 = 9437168 bits

Capacity of a 32Kx8 chip: 25 x 210 x 23 = 218 bits

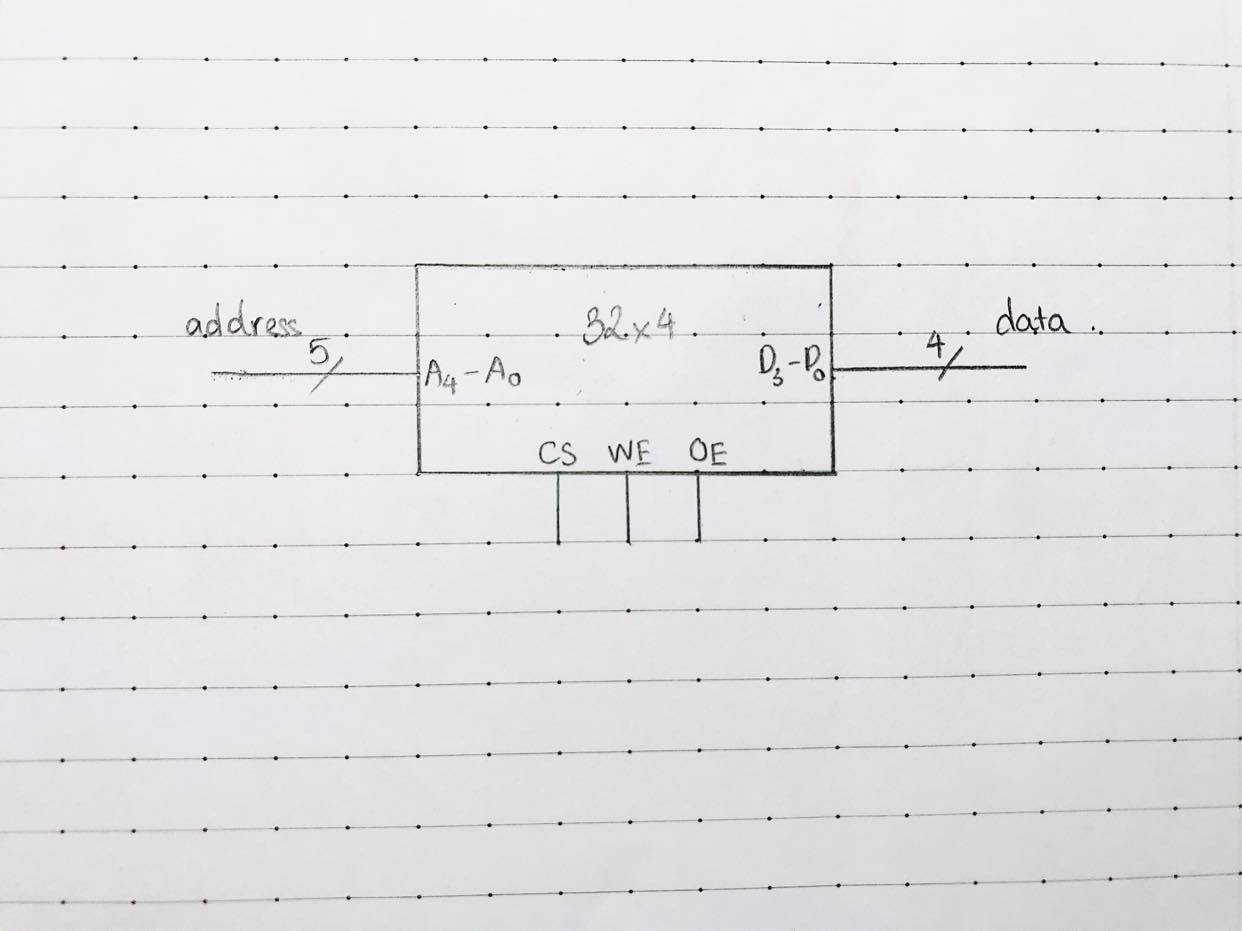
→ Number of 23Kx8 chips needed: 9437168/218 = 36 chips

Question 4

1. 32 addresses → Must have log232 = 5 address pins

Each location can store 4 bits → 4 data pins

Memory capacity = 32 x 4 (bit) = 128 bit = 16 bytes

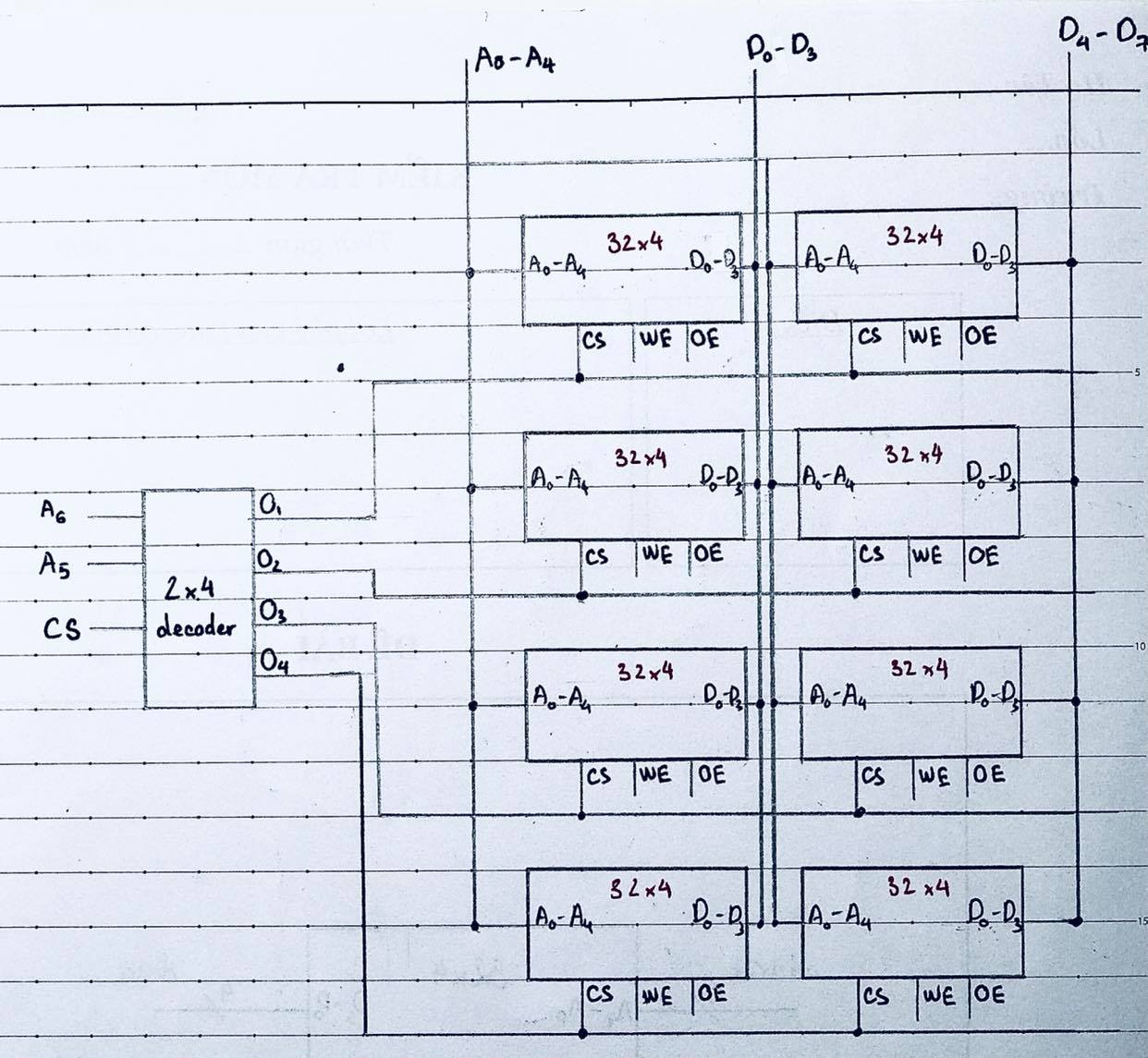


1. 32x4 memory has 32 words, each store 4 data bits

→ To make 32x8 memory (32 words, each store 4 bits), need **two** 32x4 memory arrange in a row

→ To make 128x8 memory (128 words, each store 8 bits), need in total **four** 32x8 memory arrange in one column

→ To make 128x8 memory, need 2x4 = 8 32x4 chips



128 addresses → Must have log2128 = 7 address pins

Each location can store 8 bits → 8 data pins

Capacity of the chip: 128 x 8 bit = 128 x 1 (byte) = 128 bytes

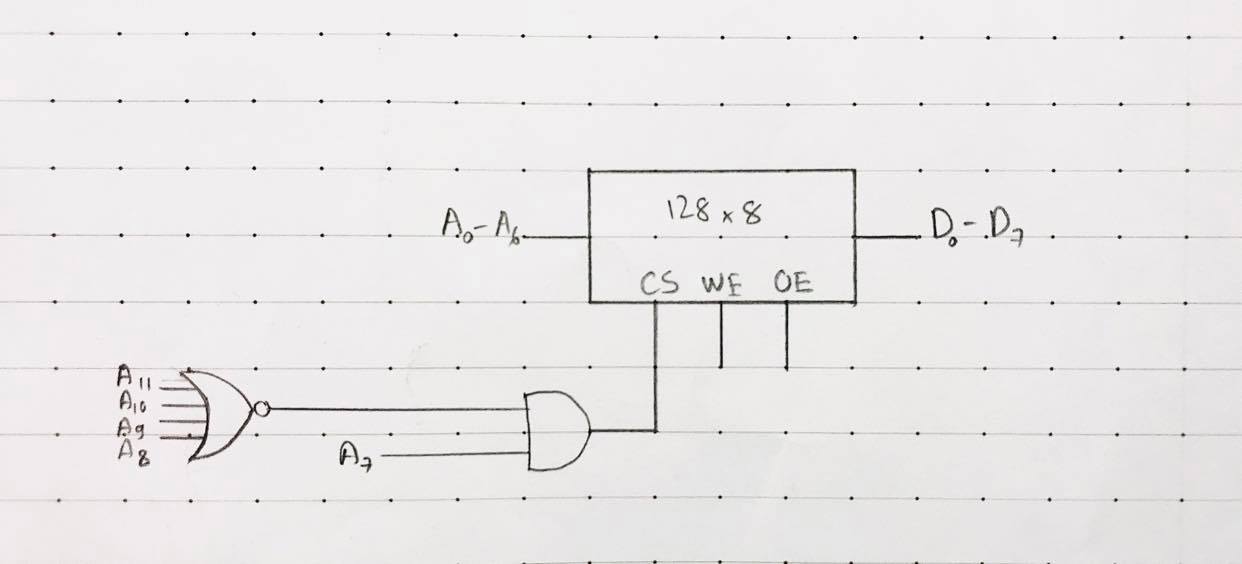
1. 080H = 0000 1000 0000

The memory is 128x8 chip → There is 27 addresses

→ Maximum address = 0000 0111 1111 = 07F

→ Address range: 080H – 07FH

→ The first five bits need to be decoded, by putting the first four bits (from the left side) through a NOR gate (equivalent to putting each bit through a converter then AND them together), then ANDed with the 5th bit



1. CPU has 12 address lines → address space (in locations) = 212

128x8 chip has 128 locations

→ Number of 128x8 chips needed to implement such CPU: 212/128 = 32 chips

Each 128x8 chips has memory capacity of 128 bytes

→ Capacity of this system: 128x32 = 4096 bytes = 4K bytes

Question 1

